What is claimed is:

1. A ferroelectric memory device, comprising:

a substrate providing a transistor;

a first insulation material with a plane surface formed on the substrate;

a storage node contact passing through the first insulation material to contact to an active region of the substrate;

a lower electrode being connected to the storage node contact and including a solid solution layer disposed at least as an upper most layer, the solid solution layer being doped with a metal element, which is induced to be in a solid solution state;

a second insulation material having a plane surface that exposes a surface of the lower electrode, encompassing the lower electrode and being formed on the first insulation material;

a ferroelectric layer covering the second insulation material including the lower electrode; and

an upper electrode formed on the ferroelectric layer.

2. The ferroelectric memory device as recited in claim 1, wherein the solid solution layer is a Pt-metal solid solution layer where a metal element is doped into a Pt layer and induced to be in a solid solution state thereafter.

3. The ferroelectric memory device as recited in claim 1, wherein the metal can be any one selected from a group consisting of Ru, Ir, Rh, Pd, Os, Ag and Au, or any two elements of the above.

4. The ferroelectric memory device as recited in claim 1, wherein the lower electrode has a stack structure sequentially deposited with an Ir layer, an IrO_2 layer and the solid solution layer.

5. The ferroelectric memory device as recited in claim 1, wherein the solid solution layer has a thickness ranging from about 100 Å to about 4000 Å.

6. A method for fabricating a ferroelectric memory device, comprising the steps of:

forming an inter-layer insulation layer on a substrate providing a transistor;

forming a storage node contact passing through the inter-layer insulation layer and then contacting to a source/drain region of the transistor;

forming a lower electrode being connected to the storage node contact and including a solid solution layer disposed at least as an upper most layer where a metal element is doped and subsequently induced to be in a solid solution state;

forming an isolating insulation layer exposing a surface of the lower electrode and encompassing the lower electrode;

forming a ferroelectric layer on an entire surface including the isolating insulation layer; and

forming an upper electrode on the ferroelectric layer.

7. The method as recited in claim 6, wherein the solid solution layer is a Pt-metal solid solution layer formed by doping a metal element into a Pt layer and subsequently obtaining a solid solution state at the step of forming the lower electrode.

8. The method as recited in claim 7, wherein the metal element can be any one selected from a group consisting of Ru, Ir, Rh, Pd, Os, Ag and Au or any two elements of the above.

9. The method as recited in claim 7, wherein the step of forming the Pt-metal solid solution layer further includes the steps of:

forming a Pt-metal solid solution layer target by inducing a metal element with a predetermined amount to be in a solid solution state at a Pt target; and

depositing the Pt-metal solid solution layer through a sputtering technique applied to the Pt-metal solid solution target.

10. The method as recited in claim 9, wherein the step of depositing the Pt-metal solid solution layer is proceeded at a temperature of about 25 °C to about 600 °C and at a

pressure of about 0.5 mtorr to 20 torr in a state of supplying a power of about 500 W to about 3 kW for generating plasma.